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Cite as:
Svensson, J., Lindahl, N., Yun, H., Seo, M., Midtvedt, D., Tarakanov, Y., Lindvall, N., Nerushev, O., Kinaret, J., Lee, S., & Campbell, E. E. B. (2011). Carbon Nanotube Field Effect Transistors with Suspended Graphene Gates. *Nano Letters*, 11(9), 3569-3575.

Manuscript received: 15/04/2011; Accepted: 17/08/2011; Article published: 24/08/2011

Carbon Nanotube Field Effect Transistors with Suspended Graphene Gates**

Johannes Svensson,[1,‡] Niklas Lindahl,[2,‡] Hoyeol Yun,[3] Miri Seo,[3] Daniel Midtvedt,[4] Yury Tarakanov,[4] Niclas Lindvall,[5] Oleg Nerushev,[6] Jari Kinaret,[4] SangWook Lee[3] and Eleanor E. B. Campbell[3,6,*]

[1]Electrical and Information Technology, Lund University, Box 118, SE-22100, Sweden.

[2]Department of Physics, University of Gothenburg, SE-41296 Gothenburg, Sweden.

[3]Division of Quantum Phases and Devices, School of Physics, Konkuk University, Seoul 143-701, South Korea.

[4]Department of Applied Physics, Chalmers University of Technology, SE-41296 Gothenburg, Sweden.

[5]Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-41296 Gothenburg, Sweden.

[6]EaStCHEM, School of Chemistry, Joseph Black Building, University of Edinburgh, West Mains Road, Edinburgh, EH9 3JJ, UK.

[‡]These authors contributed equally to this work.

[*]Corresponding author; e-mail: Eleanor.Campbell@ed.ac.uk

[**]Financial support from the Swedish Strategic Research Foundation (SSF) through project "NEM arrayer för elektronik- och fotonikkomponenter" (RE07-0004) is gratefully acknowledged. DM acknowledges funding from the European Union Seventh Framework program (FP7/2007-2013) under grant agreement no: 246026. SWL was supported by the NRF Grant No. 2008-331-C00099 and TJ Park Junior Faculty Fellowship. HY, SWL and EEBC acknowledge financial support from the WCU program of the MEST (R31-2008-000-10057-0) and OAN and EEBC acknowledge financial support from EaStCHEM.

Supporting information:
Raman spectroscopy characterisation. Electrical characteristics of a device where the graphene gate is pulled down to the substrate surface during measurement. Fabrication of suspended graphene for deflection measurements. Details of numerical and analytical calculations. This material is available free of charge via the Internet at http://pubs.acs.org

Keywords: Carbon nanotube, field effect transistor, graphene, movable gate electrode.

Abstract

Movable gate electrodes can be used in field effect transistors to improve their switching and thereby reduce the power consumption. Due to its excellent mechanical properties, graphene is well suited to be used as the gate material in such devices. By transferring and suspending graphene flakes above semiconducting carbon nanotubes (CNTs) we have fabricated novel field effect transistors with suspended graphene gates exhibiting a minimum inverse subthreshold slope of S=53 mV/dec at 100 K. The mechanical motion of the graphene gate is confirmed by using atomic force microscopy to directly measure the electrostatic deflection. Using numerical simulations, we verify that the mechanical motion leads to an improvement in switching compared to a static-gate device. Moreover, simulations indicate that when the separation between the graphene gate and the CNT is reduced, the role of mechanical motion in switching is drastically increased, enabling inverse subthreshold slopes below the thermal limit.

Main text

One of the most important figures of merit for field effect transistors (FETs) is the inverse subthreshold slope, S, which is the minimum gate voltage change required to change the current through the channel by one order of magnitude. A low S is desirable as it allows the use of a low supply voltage and therefore a low power dissipation during each switching event while still maintaining a high current ratio between the on and off states. The inverse subthreshold slope is given by

$$S = \frac{\partial V_g}{\partial \log_{10}(I_d)} = \ln(10)\frac{k_B T}{q}\frac{C_{tot}}{C_g} \qquad (1)$$

where V_g is the gate voltage, I_d the source-drain current, C_g the capacitance between gate and channel and C_{tot} the sum of all capacitances to the channel including parasitic contributions from e.g. the intrinsic quantum capacitance of the semiconductor, charge traps and source and drain electrodes[1]. Thus, for an ideal, long channel MOSFET with a thin gate dielectric, where the C_g dominates the total capacitance, S reaches the lower thermal limit of 2.3 $k_B T/q$ which equals 60 mV/dec at room temperature. Even though conventional MOSFETs are restricted by the thermal limit, there have been several demonstrations of novel FETs that exhibit an S lower than the thermal limit by relying on impact ionization[2], band-to-band tunneling[3, 4] and movable gate electrodes[5] as well as suggestions to reduce S by using a ferroelectric gate insulator[6].

The conductivity (σ) of a semiconductor depends on the carrier density (n), which can be controlled by the voltage applied to a gate electrode (V_g). For a change of carrier density, Δn, the conductivity changes by $\Delta\sigma$

$=d\sigma/dn\cdot\Delta n$. Since $n=C_gV_g$ where C_g is the capacitance per unit length between the semiconductor channel (here the CNT) and gate and V_g is the applied gate voltage, the change in carrier density

$$\Delta n = \frac{\Delta\left(C_gV_g\right)}{e} = \frac{\Delta C_gV_g + C_g\Delta V_g}{e} \qquad (2)$$

and the resulting change in conductivity

$$\Delta\sigma = \frac{\partial\sigma}{\partial n}\cdot\frac{\left(\Delta C_gV_g + C_g\Delta V_g\right)}{e}. \qquad (3)$$

As is evident from equation 3, the induced carrier density and therefore also the conductivity can be changed either by varying the applied gate voltage or by varying the capacitance between the gate and channel. The most straightforward way to vary C_g is to change the distance between the gate electrode and the semiconductor. In this case, the first term in equation 3 can be regarded as mechanical gating which is non-zero only for a movable gate while the second term is the usual electrostatic gating. This dependence of the conductivity on mechanical motion has been used to detect the mechanical resonance of suspended CNTs[7] and graphene flakes[8] using an RF mixing technique. If the gate electrode is allowed to move, the inverse sub-threshold slope is given by

$$S = \frac{\partial V_g}{\partial\,\log_{10}(I_d)} = \ln(10)\frac{k_BT}{q}\frac{C_{tot}}{C_g + \Delta V_g\partial C_g/\partial V_g} \qquad (4)$$

implying that S will always be smaller for a transistor with a non-static gate electrode (see equations 10-18 in supporting information for a derivation of eq. 4). From equation 4 it can be inferred that $C_{tot}\approx C_g$ and a change in gate capacitance with V_g as large as possible is desirable to minimise S. By combining both mechanical and electrostatic gating by using a movable gate in a Si MOSFET, an S lower than the thermal limit has previously been obtained[5]. However, this device relied on physical contact between the gate electrode and the gate

dielectric which leads to large hysteresis. In addition relatively high voltages were needed to deflect the gate electrode due to its large mass.

Since it is difficult to use top down processing techniques to produce thin gate electrodes, low dimensional materials such as CNTs and graphene offer attractive options for suspended gate materials that allow for large deflections at low operating voltages. Numerical simulations have predicted that an *S* lower than the thermal limit can be obtained by using a suspended metallic carbon nanotube (CNT) as a movable gate electrode for a semiconducting CNT[9]. Even though we have previously demonstrated the viability of using a CNT as a non-suspended gate electrode in a carbon nanotube field effect transistor (CNTFET)[10], fabricating suspended CNT gates is difficult mainly due to the lack of positional and structural control during CNT growth. Graphene flakes are easier to locate since they have a high optical contrast on SiO_2 which simplifies device fabrication and their electronic properties are less sensitive to their structure compared to CNTs. More importantly, graphene is well suited as a moveable gate electrode due to its excellent mechanical properties exhibiting a high Young's modulus and the largest intrinsic strength of all materials[11]. In addition, the resonance frequency of suspended graphene is tunable by electrostatically or mechanically inducing tension and is predicted to be able to reach GHz frequencies for strains around 1%[8], a feature not available in traditional resonators fabricated by top down processing techniques.

Here we present results on novel FETs which have graphene flakes, acting as movable gates, suspended over semiconducting CNTs (figure 1f). These are the first FETs reported that combine the excellent electronic properties of semiconducting CNTs such as high mobility[12], capability to carry large current densities[13] and small diameter for good electrostatic control and scalability[14] with the outstanding mechanical properties of graphene such as low mass, high strength[11] and tunable resonant frequency[8] in a single device. These devices are fabricated using a graphene transfer technique, which enables us to position the flakes with high precision and suspend long gates with only a short distance between graphene and CNT, a feature critical for low voltage electrostatic actuation of the gate and high efficiency of the mechanical gating. Electrical characterisation confirms that the suspended graphene gate can modulate the conductance of the CNT. In addition, the deflection of graphene due to the electrostatic force from the back gate is measured using an atomic force microscope (AFM). This is the first reported measurement of the magnitude of the deflection of electrostatically actuated single layer graphene since previous AFM studies only have measured small vibrations in single layered graphene[15] or the deflection of thick multilayered graphene[16]. Further, numerical simulations of the electrical characteristics of our CNTFETs illustrate the improvement gained by the mechanical movement of the gate and give guidelines for further scaling of the device dimensions.

The devices consist of individual semiconducting single walled CNTs (SWCNTs) which can be electrostatically gated either by the highly doped Si substrate with 300 nm SiO_2 gate dielectric or by a graphene flake suspended above a central segment of the CNT (figure 1f). The Si back gate is used to modulate the conductance of the segments of the CNT closest to the contacts through electrostatic doping. The

graphene gate is suspended by support electrodes and can be electrostatically deflected downwards by applying a voltage difference between the graphene and the back gate. In addition, there are also electrodes on both sides of the CNT that can be used to deflect the graphene flake electrostatically (these were not used for the reported devices).

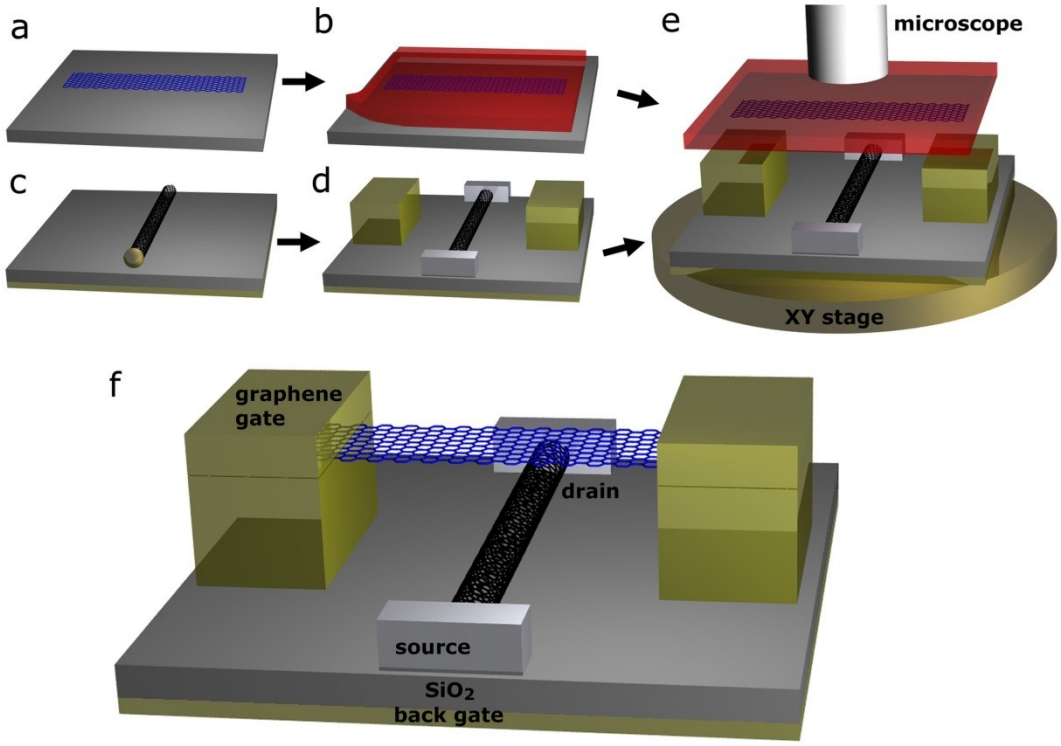

Figure 1. Schematic process for the fabrication of a CNTFET with a suspended graphene gate without any Si_3N_4 protective layer. a) Graphene flake deposited on a Si/SiO_2 substrate is located using an optical microscope. b) PMMA is spun on the substrate and released together with the graphene flake. c) CNTs are grown from Fe catalyst particles. d) Contacts and support electrodes are patterned using EBL. e) A graphene flake is aligned and suspended above the CNT using a translational stage. f) The graphene flake is finally clamped on top. The CNTFET can be gated by either the suspended graphene gate or by the Si substrate acting as a back gate.

SWCNTs were synthesized by chemical vapour deposition (CVD) at 900°C and atmospheric pressure using methane as the carbon precursor and a patterned film of 1 nm Fe on 5 nm Al_2O_3 as catalyst (figure 1c)[17]. The SWCNTs were grown on a highly-doped Si substrate with a 300 nm thick thermal oxide, a thickness chosen to enhance the optical contrast of graphene[18]. Isolated SWCNTs were located using scanning electron

microscopy and contact electrodes (0.5 nm Ti / 25 nm Pd) were patterned using electron-beam lithography (EBL). On some samples, a 15 nm Si_3N_4 protective layer was deposited on top of the CNTs using plasma enhanced CVD. Since the entire substrate is covered by the Si_3N_4 a CF_4 plasma was used to etch openings to the contact electrodes using a resist mask defined by EBL to enable electrical measurements. Next, support electrodes (5 nm Ti / 95 nm Au / 20 nm Pd) for the suspended graphene, were patterned by EBL with the SWCNT located in the middle of a 2 μm gap between the electrodes (figure 1d). The semiconducting CNT on each chip which had the lowest resistance and highest on/off ratio was identified by measuring the transfer characteristics using the Si substrate as a back gate. By sweeping the voltage on the support electrodes while measuring the current through the CNT it was also ensured that the support electrodes can not act as efficient gates. The gating effect from the support electrodes is typically small due to the 1 μm distance to the CNT and the low dielectric constant of air.

Graphene was mechanically exfoliated from highly oriented pyrolytic graphite and deposited on a silicon substrate with 300 nm oxide[19]. An optical microscope was then used to locate a graphene flake with a suitable shape to be used as a suspended gate (figure 1a). Subsequent transfer of the graphene to a substrate with a CNTFET was performed by first spincoating and baking a 500 nm thick PMMA film on the substrate thus embedding the graphene-sheet from the top (figure 1b)[20]. Immersion of the substrate into KOH released the PMMA film together with the embedded graphene. The released PMMA film was transferred to a substrate with a CNTFET using a translational stage attached to a microscope (figure 1e). During transfer, the selected graphene flake embedded in the resist film was aligned so that it was positioned between the support electrodes before it was brought into contact with the CNTFET substrate.

On some devices the transferred resist film was used in an EBL process to pattern metal patches (0.5 nm Ti / 30 nm Pd) onto the graphene segments that were on the support electrodes to ensure good electrical and mechanical contact to the graphene. The PMMA film was finally removed using acetone and critical point drying to obtain a suspended graphene flake and avoid collapse due to surface tension. The resulting device consisting of a flake of single layer graphene suspended between electrodes above a CNTFET was finally inspected using an optical microscope and an AFM. Raman spectroscopy has also been used on selected devices to determine whether the transferred graphene was single- or multi-layered (figure S1 in the supporting information).

Five CNTFETs which have suspended single or multilayer graphene flakes that can efficiently be used as gates have been successfully fabricated. A typical device with a multilayer graphene gate is depicted in figure 2. An aspect ratio as large as 20 between graphene gate length and support electrode height has been obtained while still achieving suspended graphene.

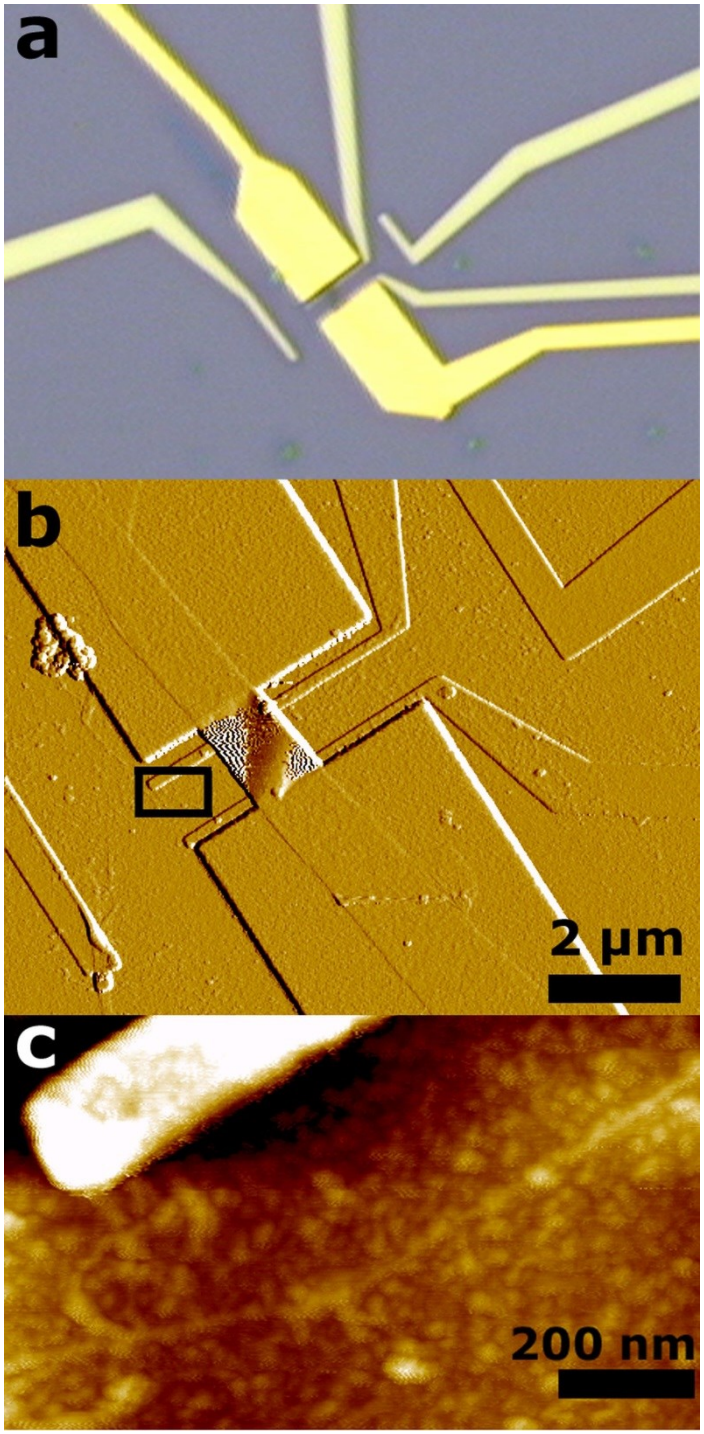

Figure 2. a) Optical microscopy image of a device with a few-layer suspended graphene strip. The wider electrodes are supporting the graphene over the CNT positioned in the gap between them. The suspended graphene region appears slightly darker in the image. b) AFM amplitude image of the device. The thinner electrodes situated in the gap between the thicker contact electrodes were intended for electrostatic deflection of the graphene gate but were not used during the measurements. c) AFM topography image of the CNT in the area indicated in b).

The devices were electrically characterized in vacuum ($5 \cdot 10^{-6}$ mbar) in a cryogenic probe station at 100 K (unless otherwise stated) by applying a source-drain bias (V_d) between the CNT contacts and either sweeping the voltage applied to the graphene gate (V_{gg}) or the back gate voltage (V_{bg}) while keeping the other gate at a fixed voltage. Contour maps for two devices are shown in figures 3a and 3c and show the improved switching when using the movable graphene gate. The contour map of the source-drain current (I_d) of a Si_3N_4 coated device with a single layer graphene strip as a gate and a graphene-CNT distance of 120 nm illustrates that the CNTFET is n-type with a high electron current at positive gate voltages and negligible hole current at negative gate voltages (figure 3a). Pd contacted CNTs exposed to air usually display p-type behaviour but the Si_3N_4 coating process either changes the contact work function or the doping of the CNT, resulting in n-type behaviour[21].

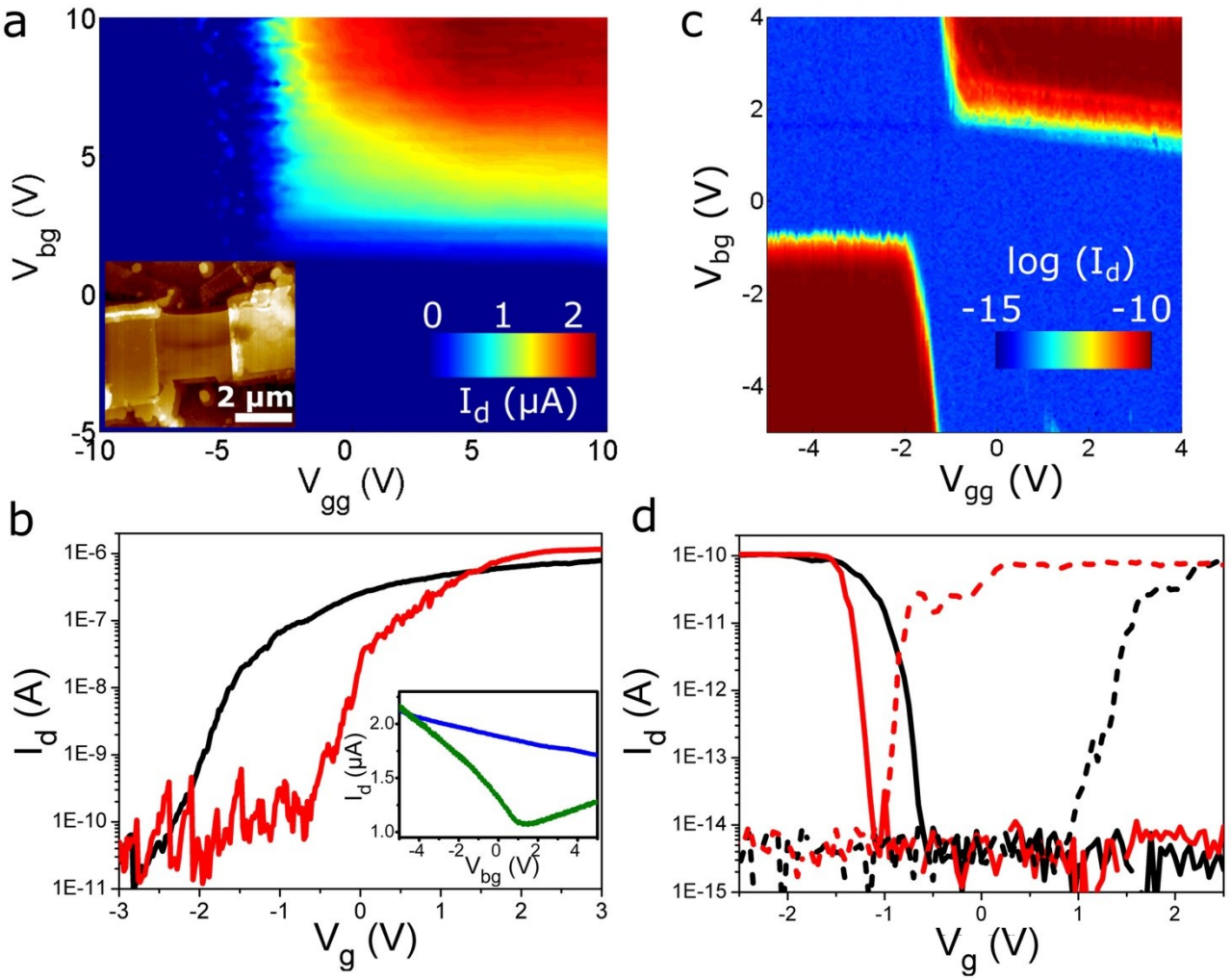

Figure 3. a) Contour plot of I_d as a function of V_{bg} and V_{gg} at V_d= 100 mV and 100 K for a device with a single layer suspended graphene gate and with Si_3N_4 coating on the CNT. V_{bg} was swept down to -10V without any measurable hole current. Inset: AFM height image of the device with the suspended graphene gate in the

central part. There are some resist residues remaining close to the device and the CNT can not be imaged due to the non-conformal coating of the Si_3N_4 layer. b) Transfer characteristics with V_{bg} (black) and V_{gg} (red) sweeps at V_d= 500 mV and 100 K for the device in a). The gate which is not swept is held at 10V. Inset: IV_{bg} characteristics of the suspended graphene gate at 300 K in air (blue) and 80 K in vacuum (green) with V_d=5 mV. There is a large negative shift of the Dirac point when the device is put in vacuum, most likely due to the removal of adsorbents that dope the graphene[22]. c) Contour plot of I_d as a function of V_{bg} and V_{gg} at V_d= 100 mV and 78 K for the device in figure 2 which has a multilayer graphene gate. d) Transfer characteristics with V_{bg} (black) and V_{gg} (red) sweeps at V_d= 100 mV and 100 K with the gate which is not swept kept at either -5V (solid lines) or 4 V (dashed lines) for the device in c).

When both V_{bg} and V_{gg} are kept at sufficiently high positive voltages the entire CNT is electrostatically n-doped with a high conductance. However, if V_{bg} is too low, the bands in the segments of the CNT close to the source and drain contacts are shifted up which prevents an electron current from passing through the CNT. Since the Schottky barriers at the contacts prevent a large hole current, the conductance is suppressed. Likewise, a low V_{gg} shifts the bands upwards in the central region of the CNT thus inducing a potential barrier that suppresses the conductance, irrespective of V_{bg}. The CNTFET depicted in figure 3a has an on/off ratio of 10^4 and a minimum resistance of 90 kΩ. The 2.1 µm wide graphene gate, which is clamped on top by Pd, has a maximum resistance of 4.7 kΩ at the Dirac point (inset in figure 3b) and its conductance can be modulated by the back gate. The Dirac point shifts towards V_{bg}=0 V when put in vacuum, but the maximum resistance still occurs at a positive V_{bg} and the transfer characteristic is asymmetric with a higher hole current. This indicates that even though the doping of the graphene changes considerably due to removal of adsorbents there are still some p-dopants remaining[22].

Single sweeps of V_{bg} and V_{gg} while keeping the other gate voltage fixed at 10 V exhibit inverse subthreshold slopes of S=317 mV/dec and S=286 mV/dec respectively (figure 3b). A second device with multilayered graphene, but without the Si_3N_4 coating, exhibits ambipolar behaviour with high conductance at both positive and negative voltages (figure 3c) and an S=66 mV/dec for the p-type branch both for the V_{gg} and the V_{bg} sweeps (but with V_{gg} retaining this slope over four orders of magnitude in current range, figure 3d) and an S=53 mV/dec for the V_{gg} and S=130 mV/dec for the V_{bg} sweeps in the n-branch. The higher S for the coated device could be due to charge traps present in the Si_3N_4[23] resulting in an additional contribution to the parasitic capacitance (see equation 4). As either V_{bg} or V_{gg} is swept, the graphene is deflected due to the attractive electrostatic force $F=1/2\ dC/dz\ |V_{bg}-V_{gg}|^2$ where C is the capacitance between the graphene and the back gate and z is the direction normal to the substrate surface. Although the graphene gate will be deflected during the V_{bg} sweep, this should not influence the transport through the nanotube since the voltage applied to the graphene gate is chosen not to introduce a potential barrier in the channel. The influence of the moving gate should only be apparent when V_{gg} is swept. For the single-layer graphene device, the presence of the

moving gate reduces the inverse sub-threshold slope by ca. 10%. In the multilayer device the reduction in the n-branch is as much as 60%.

Since it is not possible to deduce how much the graphene gate is moving only by studying the electrical characteristics, deflection due to electrostatic gating of a single layer graphene beam was also measured using an AFM (more details on sample fabrication for the AFM measurements can be found in the supporting information). The measurement technique is similar to that of Lefévre et al.[24], where an AFM operated in non-contact mode was used to measure the deflection of a multiwalled CNT under electrostatic gating. After locating the suspended single layer graphene beam, the conductive tip was positioned in its center while keeping the feedback loop on to maintain the same vibration amplitude of the AFM cantilever. To minimize any tip-sample interaction that may influence the position of the graphene, the cantilever was driven to oscillate with high amplitude and the tip and the graphene are grounded while sweeping V_{bg}. Since the tip follows the position of the graphene, the deflection as a function of V_{bg} is obtained (figure 4). The deflection curve has close to quadratic dependence on V_{bg} at low voltages but a weaker dependence at higher voltages as expected[24] and the graphene deflects 37 nm at V_{bg}= 10 V (figure 4). The maximum gate voltage difference of V_{gg}-V_{bg}=20 V applied during the electrical measurements of the CNTFETs (figure 3a) should thus be sufficient to move the graphene gate a considerable part of the total distance to the CNT. In one CNTFET, a V_{gg}-V_{bg}=21 V was sufficient to irreversibly pull-down the graphene gate to the substrate (figure S2 in supporting information) which further supports the conclusion that the graphene is deflecting during the electrical measurements.

Devices with (without) Si_3N_4 measured at room temperature in air exhibit a large negative (positive) threshold voltage (V_{th}) (figure S2 in supporting information) and therefore a higher gate voltage is needed to switch off the devices at room temperature compared to at cryogenic temperatures. The high V_{th} in combination with the increased S at higher temperatures results in a risk of pulling down the graphene gate to the substrate surface during room temperature measurements which is the reason the electrical characteristics in figure 3 have been measured at 100 K. The significant reduction in V_{th} at low temperatures could be due to removal of absorbents or freeze-out of charge traps. Thus, some passivation of charge traps may be needed in order to reduce V_{th} and enable room temperature operation in air without pull-in of the graphene gate.

Even though we have confirmed that the graphene gate is deflecting, a quantitative measure of the improvement of S caused by this movement is very difficult due to the correlation between $|V_{bg} - V_{gg}|$ and the position of the graphene membrane. Therefore, we have performed self-consistent numerical simulations to determine the influence of the position of the graphene gate on the transport characteristics of the CNTFET. The simulations comprised simultaneous evaluation of the electrostatic force and carrier occupation in a semiconducting SWNT using the boundary element method and the deflection of the graphene gate using the finite element method (see supporting information for a detailed description of the simulations). The simulated electrostatic deflection of the graphene gate was fitted to the deflection curve in figure 4. This allowed us to

extract an initial strain of $3 \cdot 10^{-4}$ in the graphene membrane which agrees well with previous experimental observations[8].

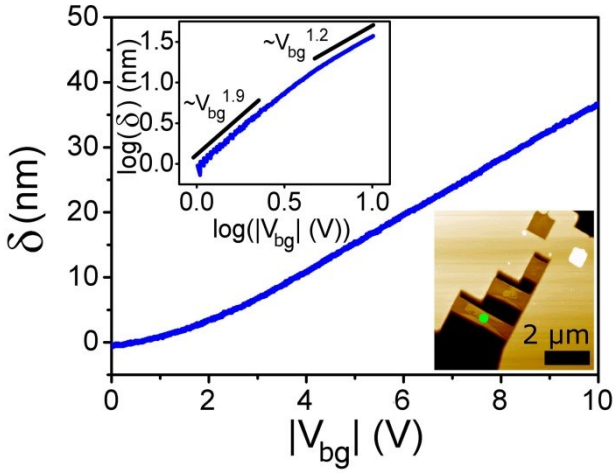

Figure 4. Deflection of the center of a 2.9 µm long suspended graphene beam as a function of V_{bg} measured using AFM. Upper inset: data in log-log plot. Lower inset: AFM image of the test device with beams of different lengths. The dot indicates the position of the measurement.

The conductance of the CNT channel was calculated using the Drude model for the diffusive one-dimensional conductance[25] and with the charge distribution in the CNT with V_s=V_d=0 obtained from simulations. This simplified model is valid only for low bias when the charge distribution and thus conductance is not affected by the electric field along the CNT, and does not take into account the Schottky barriers on the CNT-source and CNT-drain interfaces. Nevertheless, even though the model can not be used to make quantitative comparisons with experimental results, it still gives a qualitative description of the subthreshold characteristics of a CNTFET which is useful for comparing the performances of different device geometries. The simulations were carried out for a p-doped CNT at a temperature of 300 K.

A comparison between the simulated transfer characteristics for a movable graphene gate and those for a static gate at the positions corresponding to zero and maximum deflection illustrates that there is only slight improvement in switching due to movement of the graphene gate for an intial suspension height of 120 nm (figure 5a). The value of *S* decreases as the distance between the graphene gate and the CNT is decreased, from S = 94 mV/dec for 120 nm separation to 83 mV/dec. for 100nm separation. By allowing the graphene gate to move between these two extremes, the value of S is reduced further to 65 mV / dec., an improvement of 22% compared to the static gate at the minimum separation.even although the deflection of the graphene gate is only 17% of the total distance to the CNT. The improvement gained by the mechanical motion is more pronounced in the simulations for a device with a suspension height of 20 nm (figure 5b). For such small

distances, the graphene gate deflects 50% of the distance to the CNT and a clear improvement due to the graphene movement is seen with S=27 mV/dec at 300K (dashed blue line in figure 5b) which is less than half of the thermal limit for a device with a static gate and also less than half of the values calculated for S with static gates corresponding to the maximum (20nm) and minimum (10 nm) separations.

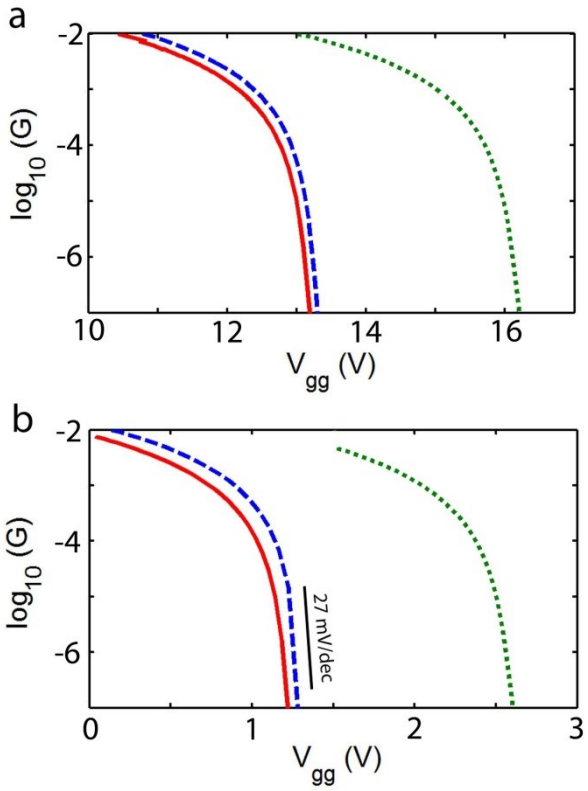

Figure 5. a) Simulated transfer characteristics at 300 K for a movable graphene gate (dashed blue line) and for a fixed CNT-graphene distance of 120 (solid red) and 100 nm (dotted green) corresponding to the initial position and the position at the maximum deflection respectively with V_{bg}=-10V. The width and length of the graphene gate were chosen to be 2.1 µm each and the initial distance to the CNT was 120 nm, in agreement with the experimental geometry for the device in figure 3a. The diameter and length of the CNT were 1.6 nm and 4 µm respectively. The conductance was normalised to the value in the on-state, corresponding to a large carrier occupation in the CNT[25]. b) Simulated transfer characteristics as in a) but with fixed CNT-graphene distances of 10 nm (solid red) and 20 nm (dotted green), displaying a strong improvement in switching and a more pronounced effect of mechanical motion of the graphene gate (dashed blue) compared to a). Note that the V_{gg} scales are different in a) and b). Details of the simulations are presented in the supporting information.

In order to get more insight into scaling of the subthreshold slope and the maximum deflection for a wide range of distances between graphene and CNT for realistic devices where parasitic capacitances are present,

we have developed an analytical coupled capacitive model for graphene deflection and CNTFET switching. This model allows the extraction of parasitic capacitances from the experimental data and the assessment of the minimum attainable S for a particular geometry and initial strain of the graphene (see supporting information). Such calculations allow us to study the performance limits of our devices and obtain guidelines for design optimisation. The results reveal that in order to obtain an *S* lower than the thermal limit for our experimental devices with 120 nm suspension height, the graphene gate has to deflect more than 80% of the distance to the CNT. At such large deflections, the electrostatic forces from the gate will overcome the elastic forces that try to restore the graphene to its equilibrium position and thus it will be irreversibly pulled in and adhere to the substrate surface. To avoid the graphene gate snapping to the surface, the distance to the CNT would have to be reduced to 3 nm due to the large influence of parasitic contributions to the total capacitance (see eq. 1). Such small distances are however difficult to realise experimentally, but the analytical calculations illustrate that by reducing the effect of parasitic capacitances such as charge trapping at the substrate surface, an initial CNT-graphene distance of 20 nm is sufficient to obtain an *S* lower than the thermal limit, which is supported by the simulations presented above.

S in the measured devices is higher than the ideal value of 20 mV/dec at 100 K mainly due to the relatively large air gap between the CNT and the graphene gate but charge traps on the substrate surface or in the Si/SiO_2 interface could also have a detrimental impact (see equation 4). To fully exploit the mechanical gating effect of the graphene gate and obtain an *S* below the thermal limit, the results of the simulations illustrate that the distance to the CNT has to be reduced and the impact of charge traps minimized. The use of two gates on opposite sides of the CNT has a detrimental effect on *S* since they compete for control of the potential in the CNT channel. Therefore, the electrostatic doping induced by the back gate should ideally be replaced by chemical doping of the CNT segments outside the region affected by the graphene gate which should further improve *S*[26].

One attractive application of nanoelectromechanical systems is mechanical resonators for on-chip clock or filtering applications[27]. Such resonators offer low power consumption, possible integration with CMOS circuits and electronic tunability of their resonance frequency by varying their strain. Graphene is suitable for such applications due to its low mass and high stiffness which enable vibrations in the GHz range and its atomic-scale thickness which results in large resonance frequency tunability with small deflections. Recently, a high Q-factor of 100000 at low temperatures with an applied tensile stress[28], has been demonstrated. Moreover, the highly nonlinear multimode graphene vibrations[29] open up the possibility of novel applications such as simultaneous mass and position sensing[30] and even for creating quantum-mechanical superpositions of mechanical states of a graphene resonator[31]. A particular drawback of nanomechanical structures is the difficulty to electronically detect their high-frequency vibrations due to their small size. Using a FET as a readout with a built-in amplification has been recognized as a strategy to achieve a sensitive readout[27, 32] as an alternative to more complicated electrical mixing[8] or optical[33] techniques, a feature important for e.g. sensitive mass sensing[8, 30, 34]. A CNTFET is a component which switches by moving only a small amount of charge[10]

and is thus very suitable as a readout of the movement of a graphene resonator. Therefore, the device presented in this study can be useful as a tunable graphene resonator with a sensitive FET readout. The high Q-factor of graphene gives a very low power operation of the resonators and the possibility to electrostatically induce tension enables devices with a highly tunable resonance frequency. Thus, such resonators are promising candidates for on-chip integration with high frequency digital or analogue circuits, acting as passive band-pass filters or as components in clock oscillators.

In summary, the use of suspended graphene as a movable gate has many advantages compared to e.g. using Si[5] due to its high stiffness and strength, low mass and the simple electrostatic tuning of the resonance frequency of graphene. In addition, the device design presented here where the suspended gate does not touch the surface during operation alleviates the problem of stiction which results in large hysteresis and can lead to mechanical failure of graphene electromechanical switches[35].

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